**COL215 Assignment 2: Design Description**

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2019CS51077

**Entitities Used**

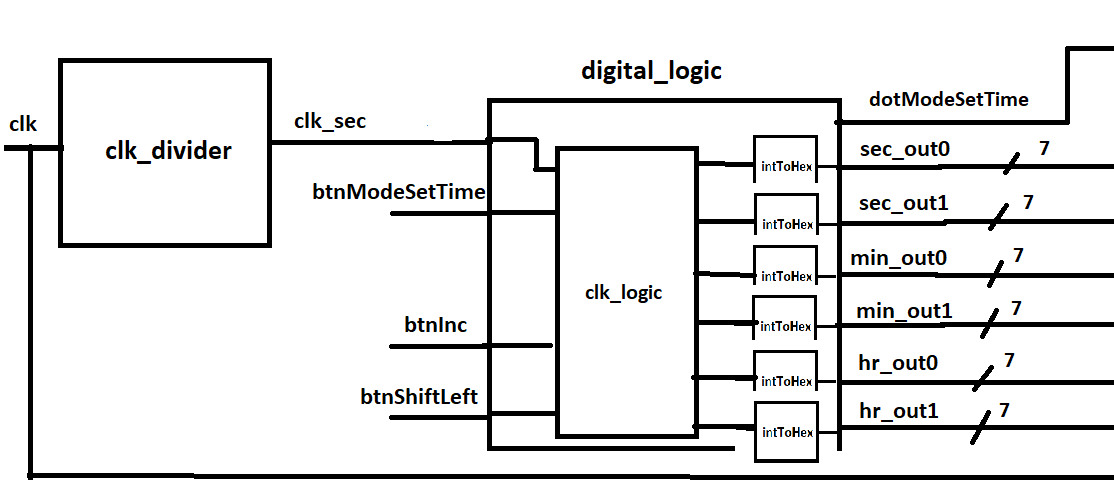
**1) clk\_divider -** it is used to get a 1 second clk from 100MHz clk

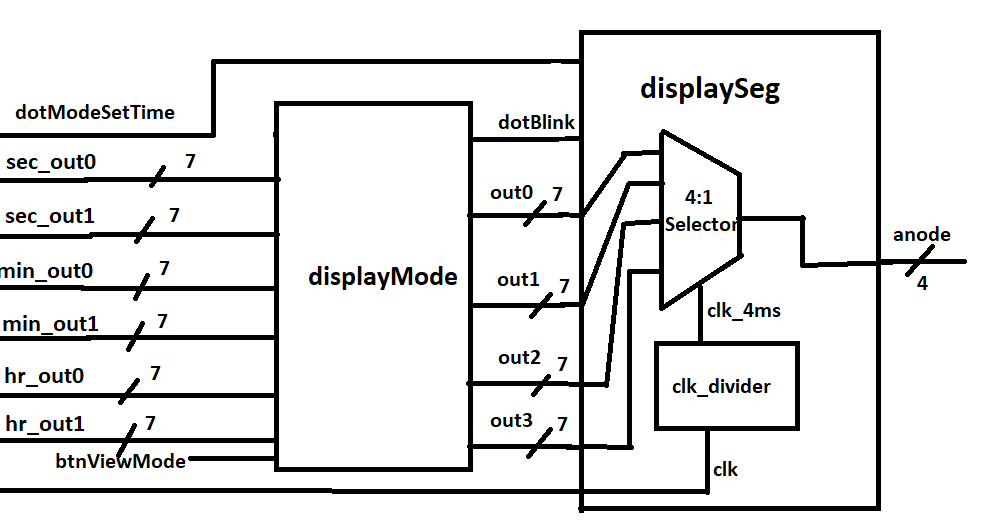
**2) digital\_clk -** it is the module that implements clock logic and setting time

**3) intToHex -** converts decimal int to hexadecimal for 7 seg display input

**4) displayMode -** implements the logic of which viewing display mode

**5) segDisplay -** displays the time and point on FPGA using 7 seg display





**Design Descisions**

**1) Buttons used -**

**a) btnModeSetTime -** toggle between set time and normal mode with each press

**b) btnShiftLeft -** shift changing field to left with each press SS->MM->HH->SS

**c) btnInc -** increase value of decimal number (23->00 and 59->00)

**d) btnViewMode -** toggle between view mode MM:SS and HH:MM with each press

2) In the set time mode the last dot/ decimal point glows to indicate the mode.

3) In the HH:MM mode, the last dot flashes at 1Hz indicating 1 second.

4) Time increment while setting time is field wise i.e SS/MM/HH.